Final

Am6080

Microprocessor System Compatible 8-Bit High-Speed Multiplying D/A Converter

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 8-bit D/A with 8-bit input data latch
- Compatible with most popular microprocessors including the Am8086 and the Am2900 Families
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current output
- Choice of six coding formats
- Fast settling current output—160 ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift—±5 ppm/°C
- Wide range multiplying capability—2.0 MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- High-speed data latch—80 ns min write time

GENERAL DESCRIPTION

The Am6080 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, chip select and other control signal lines used for direct interfacing with microprocessor buses.

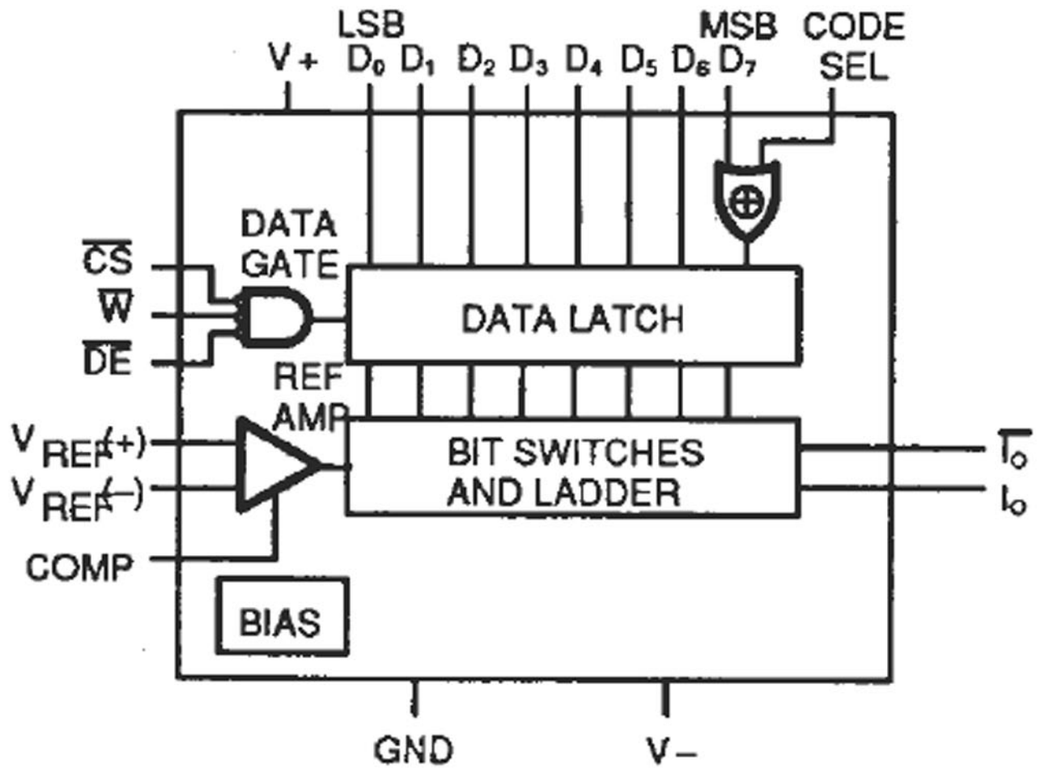
The converter allows a choice of six different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code-select input. The code control also provides a zero differential current output for two's complement coding. A high-voltage compliance, complementary current output pair is provided. The data latch is very high speed which makes the Am6080 capable of interfacing with high-speed microprocessors.

Monotonic multiplying performance is maintained over a more than 40-to-1 reference-current range. Matching within ±1 LSB between reference and full-scale current eliminates the need for full-scale trimming in most applications.

The Am6080 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power-supply voltage and temperature range.

Applications for the Am6080 include microprocessor-compatible data-acquisition systems and data-distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog-meter drivers, programmable power supplies, CRT-display drivers and high-speed modems.

BLOCK DIAGRAM



Equivalent Circuit

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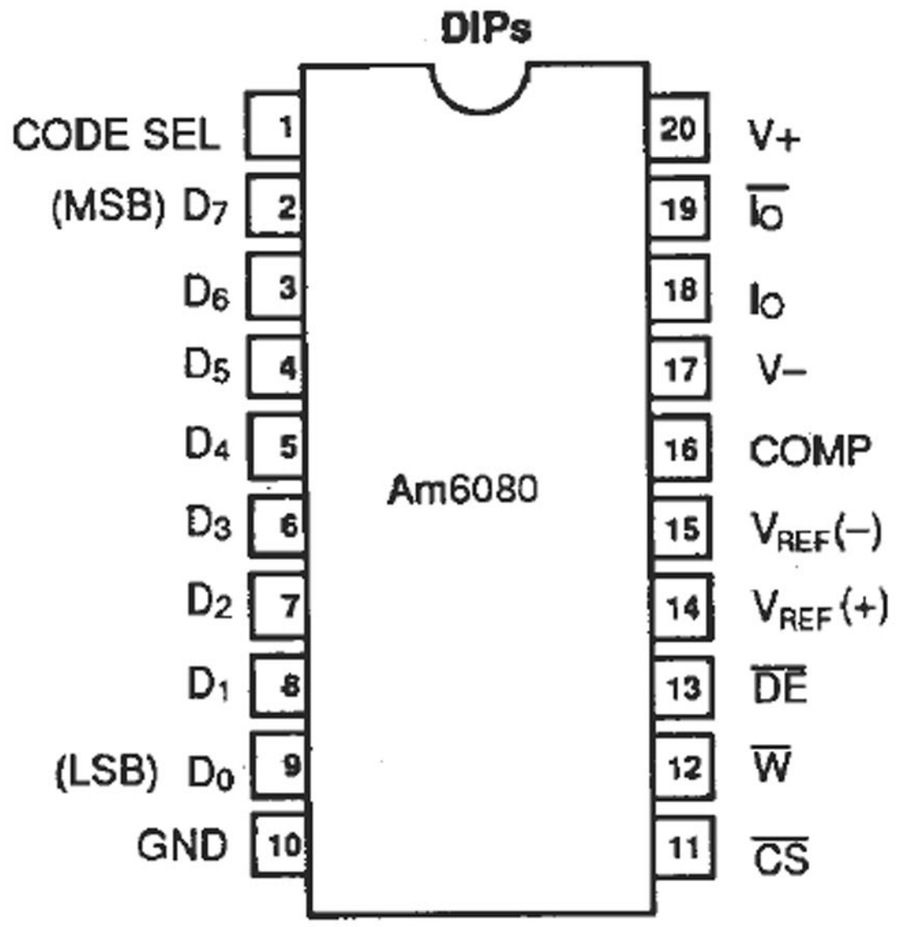
Publication # 03941 Rev. C Amendment /0

Issue Date: March 1989

CONNECTION DIAGRAM
Top View



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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**

Am6080 A D C B

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
M = Military* (–55 to +125°C)

c. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)
X = Dice

b. SPEED OPTION
A = Nonlinearity 0.1%
Blank = Nonlinearity 0.14%

a. DEVICE NUMBER/DESCRIPTION
Am6080
Microprocessor System Compatible 8-Bit High-Speed Multiplying D/A Converter

Valid Combinations	
Am6080 Am6080A	DC, DCB, PC, DMB XM, XC

*Military temperature range products are "NPL" (Non-Compliant Products List) or Non-Mil-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 4, 5, 6.

PIN DECRIPTION

D_0-D_7

D_0-D_7 are the input bits 1–8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.

$\overline{CS}$
Chip Select

This active low input signal enables the Am6080. Writing into the data latch occurs only when the device is selected.

CODE SEL
Code Select

When CODE SEL = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I}_o$ output.

COMP
Compensation

Frequency compensating terminal for the reference amplifier.

$\overline{DE}$
Data Latch Enable

This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.

I_o, $\overline{I}_o$

These are high-impedance complementary current outputs. The sum of these currents is always equal to I_{FS}.

$V_{REF(+)}$, $V_{REF(-)}$

Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.

$\overline{W}$
Write

This active low control signal enables the data latch when the $\overline{CS}$ and $\overline{DE}$ inputs are active.

FUNCTIONAL TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

X = Don't Care

CODE SELECT

CODE SEL	Function
0	MSB Inverted (Note 1)
1	MSB Non–Inverted

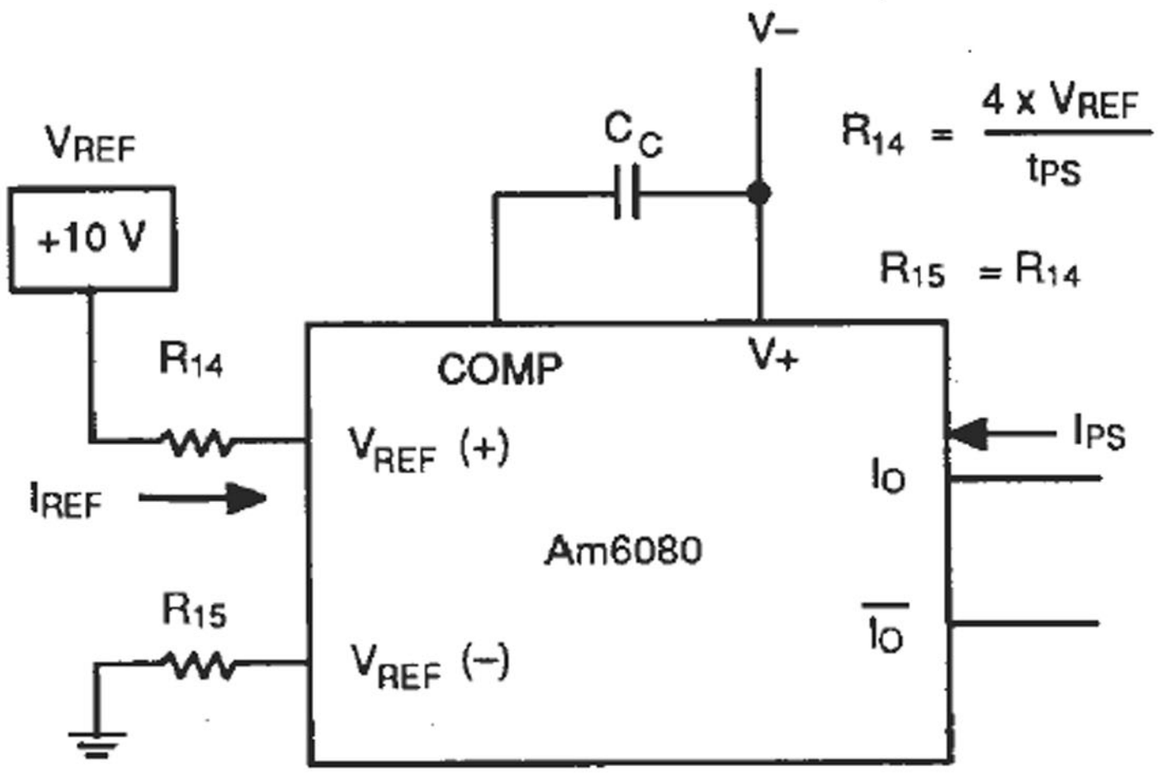
Note 1. LSB balance current is added to the $\overline{I_O}$ output.

APPLICATIONS

APPLICATION HINTS:

1. **Reference current and reference resistor.**
   There is a 1-to-4 scale up between the reference current (I_{REF}) and the full-scale output current (I_{FS}). If V_{REF} = +10 V and I_{FS} = 2 mA, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volts}}{2 \text{ mA}} = 20 \text{ k}\Omega$$



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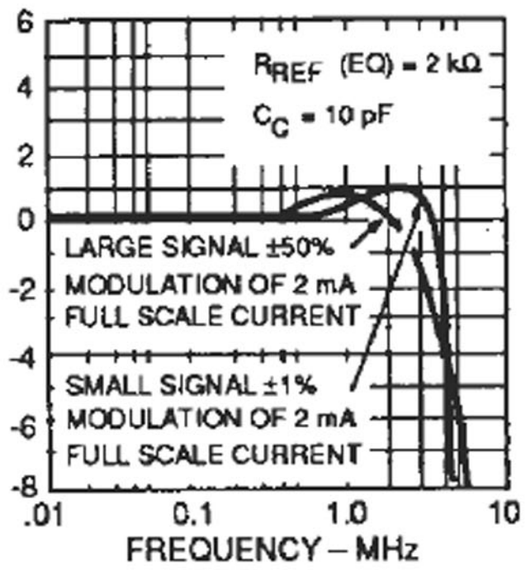
2. **Reference amplifier compensation.**
   For AC Reference applications, a minimum value compensation capacitor (C_c) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

TABLE 2.
COMPENSATION CAPACITOR
(I_{FS} = 2 mA, I_{REF} = 0.5 mA)

R_{REF} (kΩ)	C_c (pF)
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response



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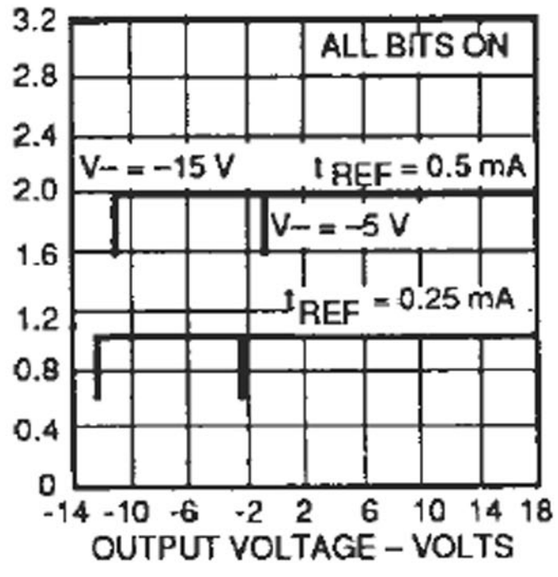
Output Voltage Compliance



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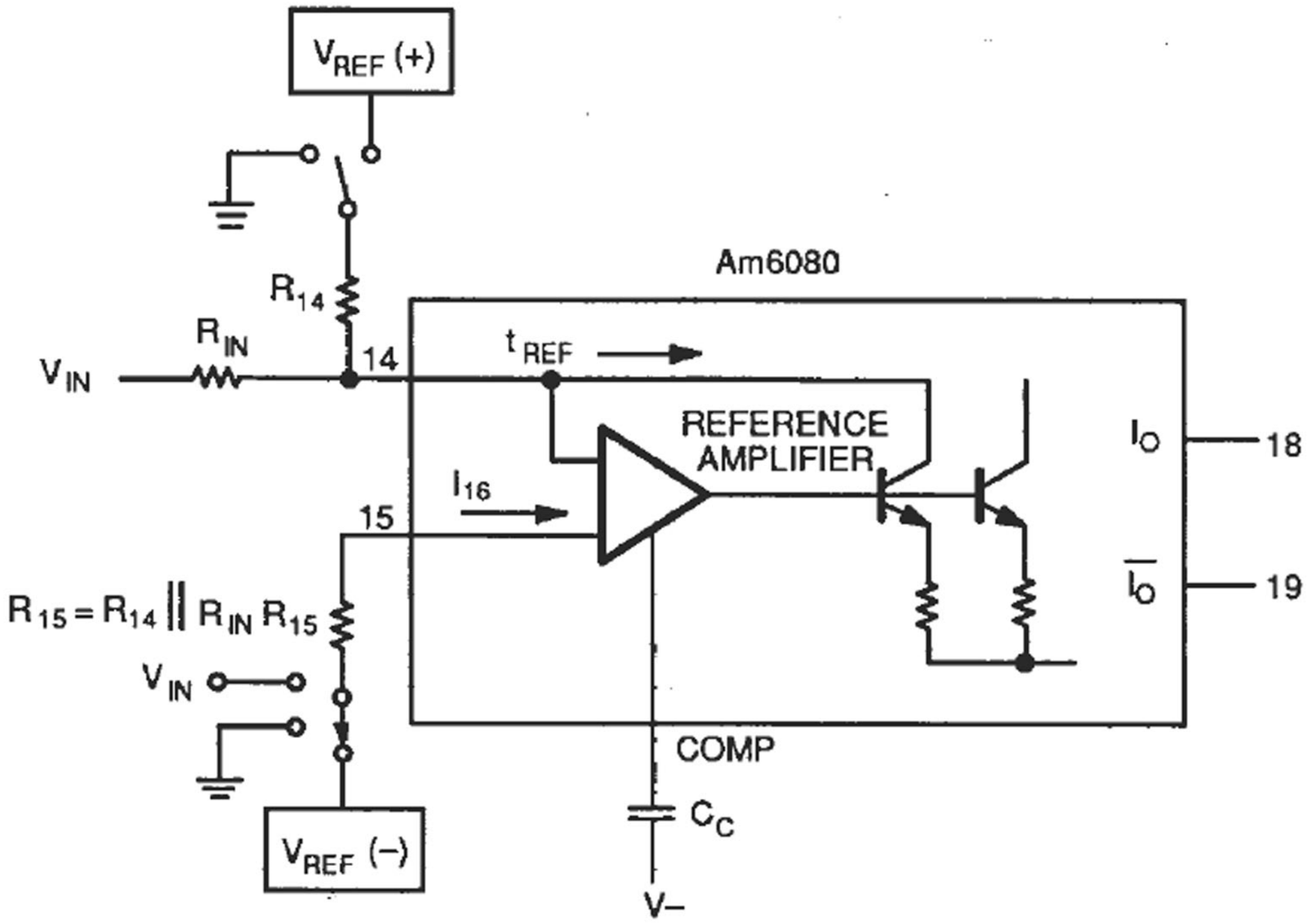
A 0.01-µF capacitor is recommended for the fixed reference operation.

APPLICATIONS (continued)



Reference Amplifier Biasing

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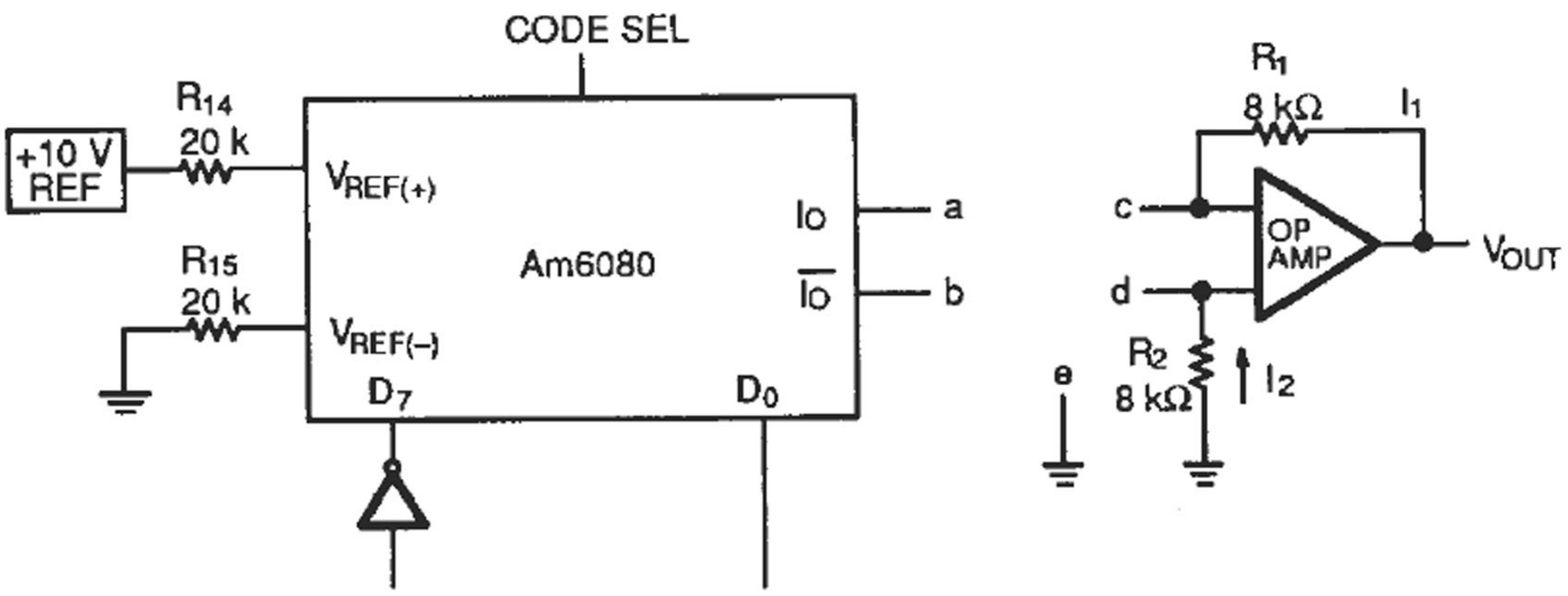
Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01 µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01 µF	$-V_{R-}/R_{14}$
Low Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
High Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_R+/R_{14}) + (V_{IN}/R_{IN})$

Notes:

1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5 pFX R_{14}(eq) in kΩ. For $R_{14} < 800\ \Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_R+/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so that the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800 Ω or less and an additional resistor may be connected from pin 14 to ground to lower the impedance.

APPLICATIONS (continued)



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CODE FORMAT		CODE SEL	CONNECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	1	a-c b-e	Positive full scale Positive full scale – LSB Zero scale	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 0 0	1 0 0	1.9929 1.964 .000	0 0 0	9.9606 9.9201 .000
	Complementary binary; one polarity with complementary input code, true zero output.	1	a-e b-c	Positive full scale Positive full scale – LSB Zero scale	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 1 1	0 1 1	1.992 1.964 .000	0 0 0	9.9606 9.9201 .000
SYMMETRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	1	a-c b-d	Positive full scale Positive full scale – LSB (+) Zero scale (–) Zero scale Negative full scale – LSB Negative full scale	1 1 1 0 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	1 0 0 1 1 0	1.992 1.984 1.000 .992 .008 .000	.000 .008 .992 1.000 1.984 1.992	9.9606 9.8807 .040 –.0404 –9.8807 –9.960
	1's complement; offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B_1).	1 (Note 1)	a-c b-d	Positive full scale Positive full scale – LSB (+) Zero scale (–) Zero scale Negative full scale – LSB Negative full scale	0 0 0 1 1 1	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	1 0 0 1 1 0	1.992 1.964 1.000 .992 .008 .000	.000 .008 .992 1.000 1.984 1.992	9.960 9.9807 .040 –.040 –9.880 –9.960
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output MSB complemented remainder add to Io (need inverter at D_7)	0 (Note 1)	a-c b-d	Positive full scale Positive full scale – LSB + LSB Zero scale – LSB Negative full scale + LSB Negative full scale	1 1 1 1 0 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	1 0 1 0 1 1 0	1.992 1.984 1.008 1.000 1.992 .008 .000	.008 .016 .992 1.000 1.008 1.992 2.000	9.920 9.840 .080 .000 –.080 –9.920 –10.000
	2's complement; offset half scale, true zero output MSB complemented.	0	a-c b-d	Positive full scale Positive full scale – LSB +1 LSB Zero scale –1 LSB Negative full scale + LSB Negative full scale	0 0 0 0 1 1 1	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	1 0 1 0 1 1 0	1.992 1.984 1.008 1.000 .992 .008 .000	.008 .016 .992 1.000 1.008 1.992 2.000	9.920 9.840 .080 .000 –.080 –9.920 –10.000

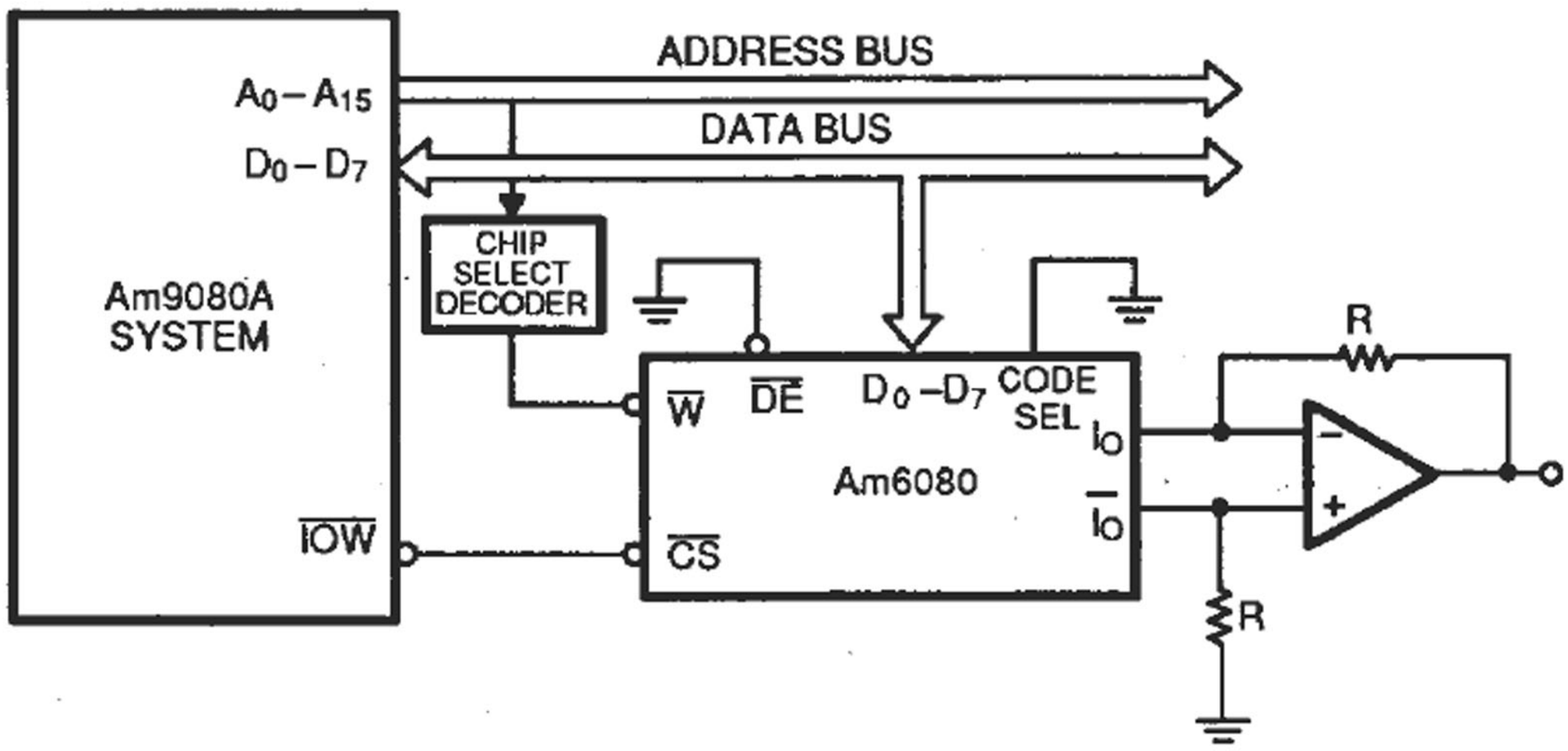
Note:

1. An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_o}$. Only one of these features is desired for this code.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

APPLICATIONS (continued)



WRITING DATA INTO THE Am6080 (2's Complement)

```
PORT 1              :EQU OOH OUTPUT PORT ADDRESS
MOV A, M            :GET DATA FROM MEMORY
OUT 0 PORT 1;       :SEND DATA
```

Am9080A Data System

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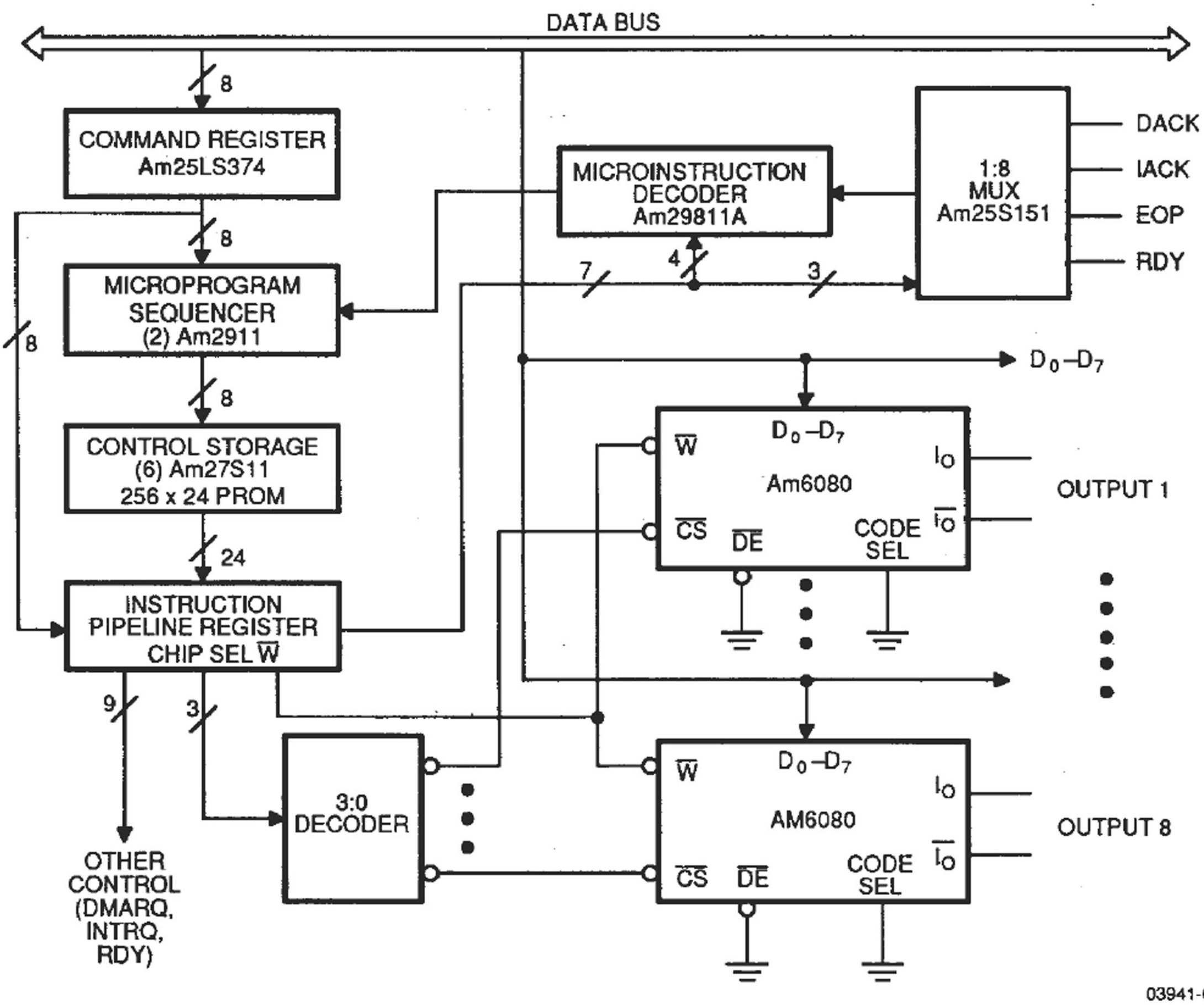

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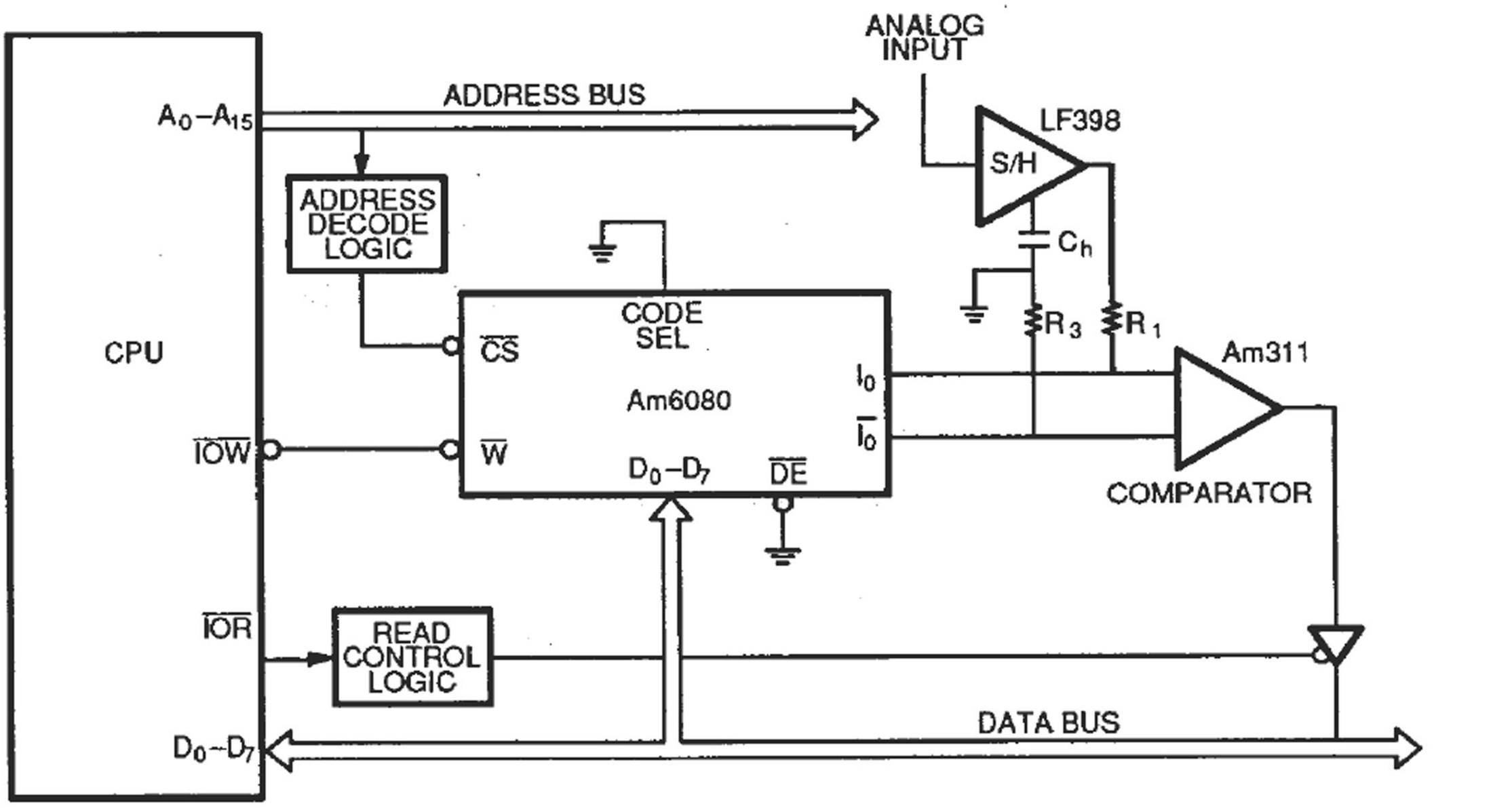
APPLICATIONS (continued)

ANALOG/DIGITAL COMVERTER UNDER SOFTWARE CONTROL



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Am6080A SOFTWARE FOR A/D CONVERSION USING Am6080

SEQ	SOURCE	STATEMENT
0 PORT1	EQU 00H	;6080 A/O PORT ADDRESS
1 PORT3	EQU 02H	;COMPARATOR ADDRESS
2	ORG 3E50H	
3 START:	LXI SP, STAKS-16	;INITIAL STAKS POINTER
4 SAMPLE:	CALL ADCON	;CALL A/D CONVERSATION
5	JMP SAMPLE	;NEXT SAMPLE
6 ADCON:	XRA A	;CLEAR ACC
7	MOV D,A	;CLEAR D REG
8	STC	;SET CARRY
9	RAR	;SET BIT 7 TO 1
10	MOV B,A	;STORE TEST BIT AT B REGISTER
11 LOOP:	MOV E,A	;STORE TEST WORD
12	OUT PORT1	;OUTPUT TO A/D
13	IN PORT3	;INPUT FROM COMP
14	CRA A	;SET SIGN FLAG
15	JM NEXT	;IF SMALLER GO TO NEXT BIT
16	MOV D,E	;SAVE RESULT
17 NEXT:	MOV A,B	;GET NEXT TRIAL BIT
18	RAR	;SHIFT RIGHT ONCE
19	RC	;RETURN ON CARRY
20	MOV B,A	;STORE TEST BIT
21	ADD D	;ACCUMULATE RESULT
22	JMP LOOP	;TRY NEXT BIT
23 STAKS:	DS 16	
24	END START	

Instrumentation and Control

Data Acquisition
Data Distribution
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

Signal Processing

CRT Displays
IF Gain Control
8 x 8 Digital Multiplication
Line Driver

A/D Converters

Ratiometric ADC
Differential Input ADC
Microprocessor Controlled ADC

D/A Converters

Signal Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC

MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Logic Inputs	–5 to +18 V
Analog Current Outputs	–12 to +18 V
Reference Inputs (V_{14}, V_{15})	V– to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18 V
Reference Input Current (I_{14})	1.25 mA

Stresses above those listed under MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military	–55 to +125°C
Commercial	0 to +70°C
Power Supply Voltage	±18 V
Die Size	0.083 x 0.121 in.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

These specifications apply for V+ = +5 V, V− = −15 V, I_{REF} = 0.5 mA, over the operating temperature range unless othewise specified. Output characteristics refer to all outputs.

Included in Group A Subgroup. 1, 2, 3, 4, 5, 6 unless otherwise noted.

Parameter	Description	Test Conditions	Am6080A			Am6080			Unit
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	bits
	Monotonicity		8	8	8	8	8	8	bits
DNL	Differential Nonlinearity		—	—	±.0.19	—	—	±.0.39	%FS
NL	Nonlinearity		—	—	±.0.1	—	—	±0.19	%FS
I_{FS}	Full Scale Current	V_{REF} = 10.000 V $R_{14} = R_{15}$ = 20.000 kΩ T_A = 25°C	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		—	±5	±20	—	±10	±40	ppm/°C
			—	.0005	±.002	—	.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	—	+18	−10	—	+18	V
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$	—	±0.1	±1.0	—	±0.2	±2.0	µA
I_{ZS}	Zero Scale Current			0.01	1.0		0.01	2.0	µA
I_{RR}	Reference Current Range	V− = −5 V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15 V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels — Logic "0"		—	—	0.8	—	—	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	—	—	2.0	—	—	
I_{IN}	Logic Input Current	V_{IN} = −5 V to +18 V	—	—	40	—	—	40	µA
V_{IS}	Logic Input Swing	V− = −15 V	−5		+18	−5		+18	V
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	µA
dI/dt	Reference Input Slew Rate	$R_{14(eq)}$ = 800 Ω (Note 2) C_C = 0 pF	4.0	8.0	—	4.0	8.0	—	mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5 V to +5.5 V, V− = −15 V	—	±0.0003	±0.01	—	±0.0005	±0.01	%FS/%
$PSSI_{FS-}$		V− = −13.5 V to −16.5 V, V+ = +5 V	—	±0.0005	±0.01	—	±0.0005	±0.01	
V+	Power Supply Range	I_{REF} = 0.5 mA, V_{OUT} = 0 V, V− = −15 V	4.5	—	18	4.5	—	18	V
V−		I_{REF} = 0.5 mA, V_{OUT} = 0 V, V+ = +5 V	−18	—	−12	−18	—	−12	
I+	Power Supply Current	V+ = +5 V, V− = −15 V	—	9.8	14.7	—	9.8	14.7	mA
I−			—	−7.4	−9.9	—	−7.4	−9.9	
I+		V+ = +15 V, V− = −15 V	—	9.8	14.7	—	9.8	14.7	
I−			—	−7.4	−9.9	—	−7.4	−9.9	
P_D	Power Dissipation (Note 1)	V+ = +5 V, V− = −15 V	—	160	222	—	160	222	mW
		V+ = +15 V, V− = −15 V	—	258	369	—	258	369	

Notes:

1. Derate Hermetic DIP 10 mW/°C above 100°C. Plastic package 6.8 mW/°C. Leadless 10 mW/°C above 100°C.
2. Not tested. Guaranteed by characterization.

AC CHARACTERISTICS

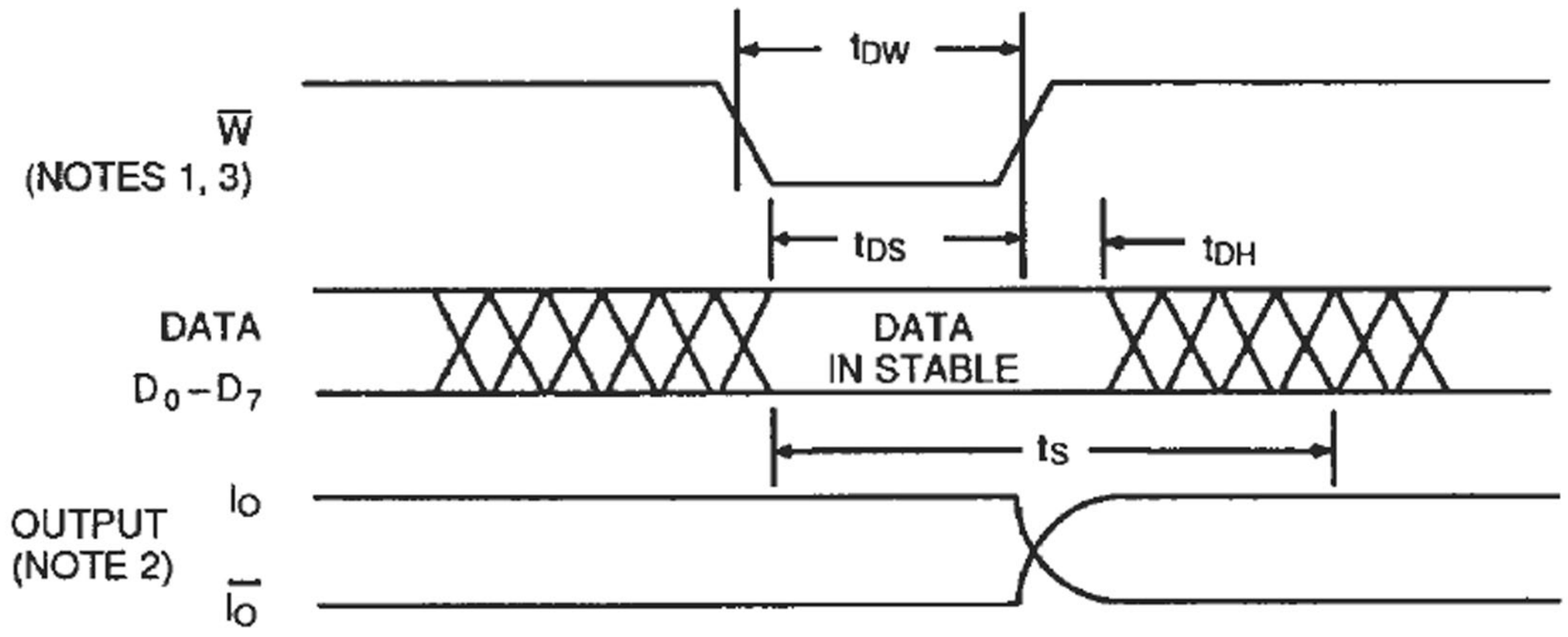
$V+ = +5$ V, $V- = -15$ V, $I_{REF} = 0.5$ mA, $R_L < 500\ \Omega$, $C_L < 15$ pF over the operating temperature range unless otherwise specified.

Parameter	Description		Conditions	Commercial			Military			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
t_S	Setting Time, All Bits Switched (Note 4)		$T_A = 25°C$ Settling to ±1/2 LSB		160			160		ns
t_{PLH}	Propagation	Each bit	$T_A = 25°C$		80	160		80	160	ns
t_{PHL}	Delay (Note 4)	All bits switched	50% to 50%		80	160		80	160	
t_{DH}	Data Hold Time (Note 4)		See timing diagram	10	–30		10	–30		ns
t_{DS}	Data Set Up Time (Note 4)		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time (Note 4)		See timing diagram	80	35		100	35		ns

Notes:

1. t_{DW} is the overlap of $\overline{W}$ LOW, $\overline{CS}$ LOW, and $\overline{DE}$ LOW. All three signals must be LOW to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. The internal time delays from $\overline{CS}$, $\overline{W}$, and $\overline{DE}$ inputs to the enabling of the latches are all equal.
4. Not tested. Guaranteed by characterization.

Timing Diagram



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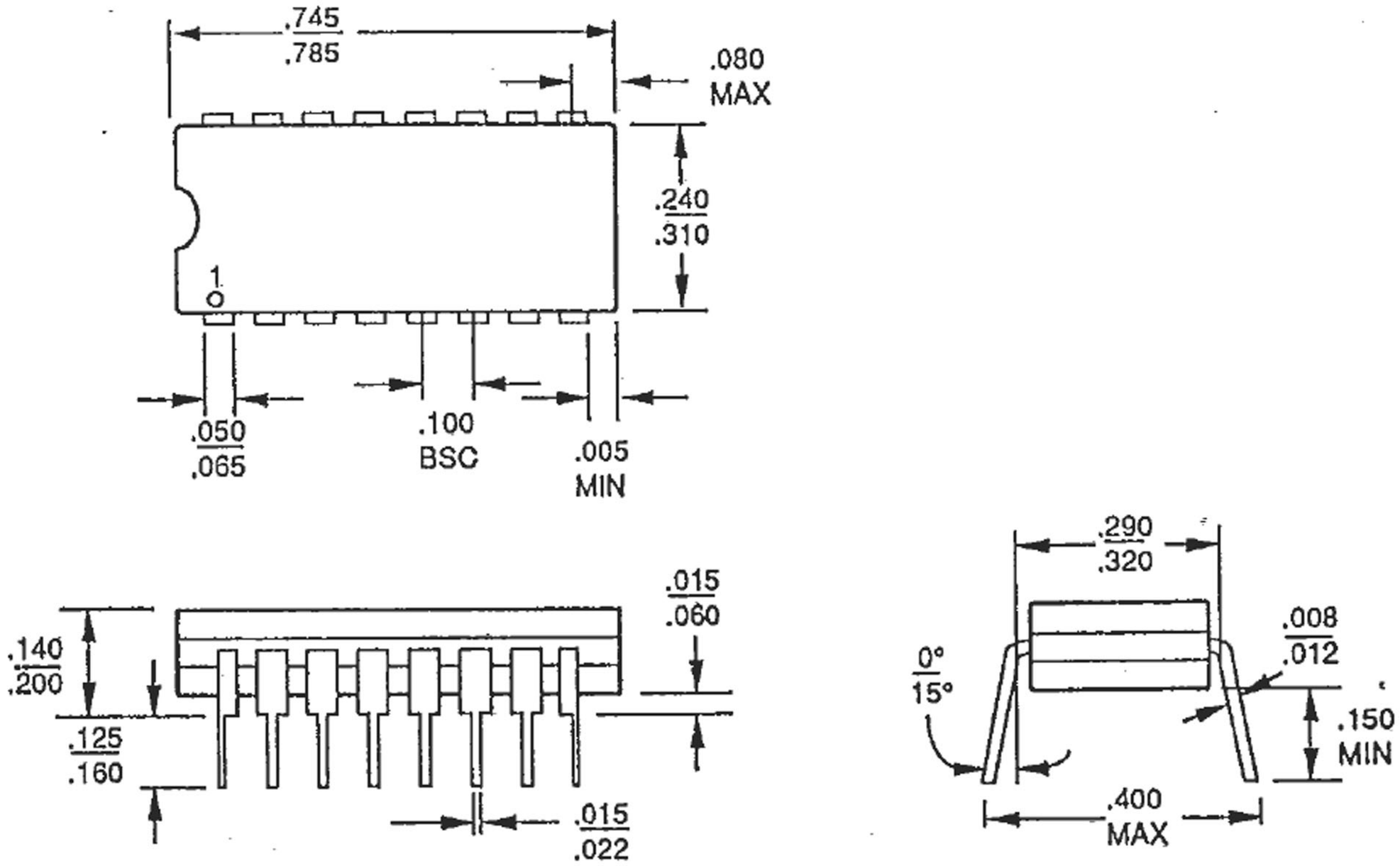
PHYSICAL DIMENSIONS
CD 016



CD 020